Amendments to the Drawings:

The attached sheets of drawings include changes to Fig. 11A and Fig. 11B (pages 7 and 8 of the Drawings). Fig. 11A is now labeled Fig. 11B and Fig. 11B is now labeled Fig. 11C.

Attachment: Replacement sheets
Annotated sheets showing changes

REMARKS

In the specification, the paragraph at lines 19 – 21 on page 13 has been amended to correct the erroneous reference to "Fig. 11A" on line 19. Line 19 now refers to Fig. 11, in accordance with the labeling on page 6/16 of the drawings and the specification in general. The amendment is clerical in nature and as such does not introduce new matter. Accordingly, its entry is respectfully requested.

In the specification, the paragraph at lines 22 – 26 on page 20 has been amended to correct the figure reference from Fig. 3 to Fig. 11C. The amendment is clerical in nature and as such does not introduce new matter. Accordingly, its entry is respectfully requested.

In order to expedite prosecution Applicants have cancelled claims 1 – 23 and added new claims 24 – 53.

Claim 24 has support throughout the specification, and, for example, the text on pages 48 to 53 of Appendix AA and the original claims. Specifically, the generalization to "different bit-sizes" has support at page 52 lines 29 to 30 of Appendix AA ("...mixed sizes of data...") and original Claim 4. The term "during different phases of neural activity" finds support at page 50 lines 30 to 33 of Appendix AA ("...depending on the phase of operation...") and page 27 lines 1 to 20 of the main description ("...different requirements at different phases of operation...").

Claims 25 through 29 are supported, respectively, by Claims 2 through 6, as originally filed.

Claim 30 relates to a neural network module, comprising the combination of an array of neural processing elements and a controller in accordance with Claim 7, as originally filed.

Claims 31 through 41 are supported, respectively, by Claims 8 through 18, as originally filed.

Claim 42 relates to a software implementation of the invention. Claim 42 is supported by the specification, for example, on page 79 lines 15 to 22.

Claim 43 relates to a method of training in neural network, is characterized by the use of different bit sizes for weight values used in steps ii. and iv. Claim 43 finds support throughout the specification, and, for example, in original Claims 3 and 4, page 27 lines 1 to 3 and lines 9 to 20 of the specification, and pages 48 to 53 of Appendix AA.

Claims 44 to 49 relate to specific embodiments of the training method.

Claim 44 is supported by the specification at page 31 lines 7 to 14. This passage refers to the importance of "additional" bits to ensure convergence during the update phase of the reference vector, thereby disclosing that the second bit-size is greater than the first.

Claim 45 is supported by, for example, the specification on page 25 line 28 to page 26 line 2.

Claims 46 and 47 are supported by Claims 3 and 4 as filed and the passage on page 27 lines 1 to 7 of the specification.

Claim 48 is supported by page 27 lines 17 to 20 of the specification.

Claim 50 relates to a software implementation of the training method. Claim 50 is supported by the specification on page 79 lines 15 to 22.

Claims 51 through Claim 51 relates specifically to a neural network trained by the method of Claim 28, and Claims 52 and 53 provide additional details of the neural network implementation.

Accordingly, new claims 24 – 53 do not introduce new matter and their entry is respectfully submitted.

In the amended figures, Figure 11A is now Figure 11B and Figure 11B is now Figure 11C.

The amendments to the claims have obviated the objections to the specification, which should therefore be withdrawn.

Turning now to the specific comments by the Examiner:

Claims 1, 2, 7, 10, 12 – 14 and 17 stand rejected under 35 U.S.C. 102(b) as being anticipated by Masuda et al. (U.S. Pat. No. 5,165,010). Applicant respectfully submits that the amendments to the claims have obviated the rejection and respectfully request that it be withdrawn.

Applicant respectfully submits that the claims have been amended to reflect the fact that different bit sizes are used for the weight values during different phases of neuronal activity. This feature is not disclosed in Masuda et al. Accordingly, Applicants respectfully submit that the rejection be withdrawn.

Claims 20 – 21 stand rejected under 35. U.S.C. 102(b) as being anticipated by Boulet et al. (EP 0 694 852 A1). Applicant respectfully submits that the amendments to the claims have obviated the rejection and respectfully request that it be withdrawn.

Applicant respectfully submits that the claims have been amended to reflect the fact that different bit sizes are used for the weight values during different phases of neuronal activity. This feature is not disclosed in Boulet et al. Accordingly, Applicants respectfully submit that the rejection be withdrawn.

Claims 3 – 6 stand rejected uunder 35 U.S.C. 103(a) as being unpatentable over Masuda et al. (U.S. Pat. No. 5,165,010) in view of Adelman et al. (EP 0718 757 A2).

Applicants respectfully disagree and request that the rejection be withdrawn for the following reasons.

Applicants respectfully submit that Masuda et al. would not lead the skilled artisan to adopt an approach that used different bit-sizes for the weights of a single neuron. Furthermore, the skilled person would not look to the field of DSP in general, and to consider the teachings of the Adelman et al document, to be correct. Accordingly, the deficiencies of Masuda are not made up for by teachings of Adelman.

The Adelman et al. reference discloses a method and apparatus for Digital Signal Processing (DSP) applications. In Adelman, there is provided a data-bit size indicator means in a DSP chip which allows the chip to perform operations on different bit-size data values using the same instruction set. The example given in the Adelman document is use of 16-bit values and 24-bit values in GSM and digital audio applications respectively. The motivation for the Adelman system is to provide hardware capable of carrying out a number of different DSP operations.

In contrast, the claimed invention is concerned with a neural processing element and associated apparatus and methods. The claimed invention is characterized by the use of different bit-size data for the weight values during different phases of neural operation. One motivation for using different bit-size data is to guarantee convergence during the training process. This is expressed, for example, in paragraph 2 of page 31 of the specification.

When seeking to provide an improved neural network processor and associated methods, and, in particular, to seek convergence during a training process, one skilled in the art would not turn to the more general field of DSP to seek a solution. Furthermore, from the field of DSP, Adelman would only be selected as a relevant document with the benefit of hindsight, i.e. after the skilled person had identified that using data different bit-sizes was of benefit to the neural processing application.

Even if the skilled artisan did have regard to Adelman, he would not assume from its teachings that the use of different data bit-sizes is appropriate for the weights of a single neuron of a neural network of the type disclosed in Masuda. In fact, the skilled artisan would be motivated to

keep the design of neural processing element as simple as possible, and would not seek to introduce additional complications to the processing and hardware that are required to use different bit-sizes for the weight values.

The skilled artisan would not therefore consider the disclosure of Adelman, and in any case would not be motivated to apply its teachings to weight values of a single neuron in a neural network. Accordingly, Applicants respectfully submit that the rejection be withdrawn.

Claims 8, 9, 11, 16 & 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masuda et al. (U.S. Pat. No. 5,165,010) in view of Crosetto (U.S. Pat. No. 5,937,202).

Applicants respectfully disagree and request that this rejection be withdrawn for the following reasons.

Applicants respectfully submit that Matsuda et al. would not render the claimed invention obvious for the reasons outlined above. Furthermore, the deficiencies of Matsuda et al. are not made up for by the teachings of Crosetto. Accordingly, Applicants respectfully submit that the rejection be withdrawn.

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Masuda et al. (U.S. Pat. No. 5,165,010) in view of Huppenthal et al. (U.S. Pat. No. 6,247,110).

Applicants respectfully disagree and request that this rejection be withdrawn for the following reasons.

Matsuda et al. would not render the claimed invention obvious for the reasons outlined above. Furthermore, the deficiencies of Matsuda et al. are not made up for by the teachings of Huppenthal et al. Accordingly, Applicants respectfully submit that the rejection be withdrawn.

In view of the foregoing it is respectfully submitted that all claims are in condition for allowance. Early and favorable action is requested.

If any additional fee is required, charge Deposit Account No. 50-0850.

Date: 12/16/05

Respectfully submitted,

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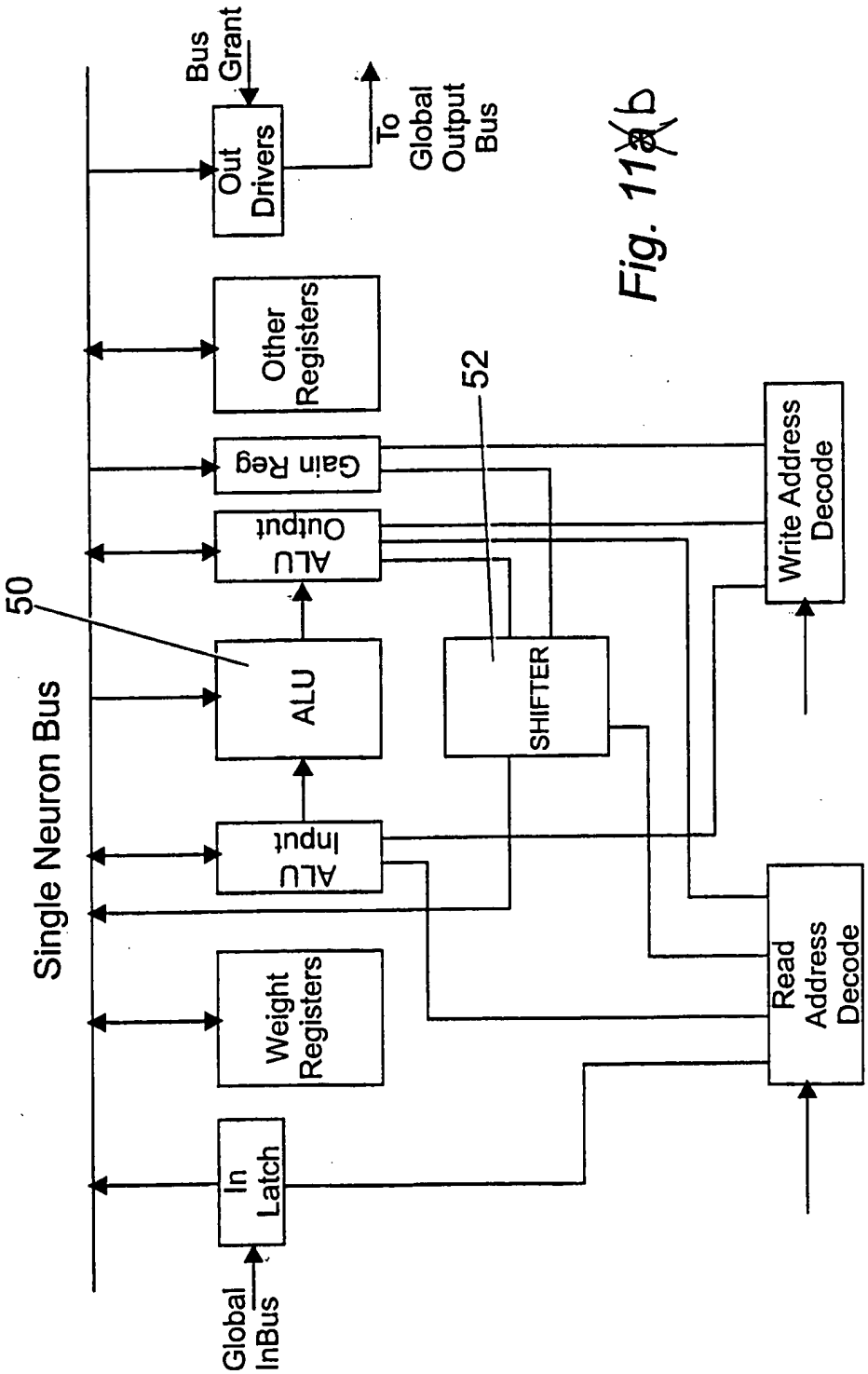

Fig. 11b

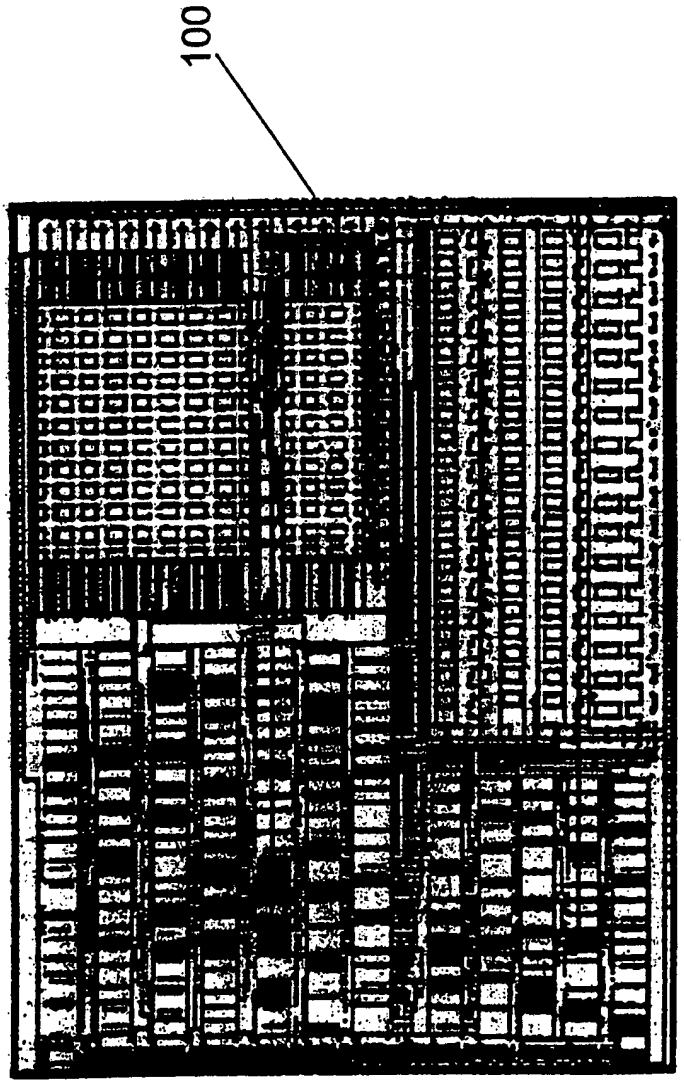

Fig. 11b/c